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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,075	06/27/2003	Fu-Shiung Hsu	MXIC-P910322	7496

7590 05/28/2004

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/609,075	HSU ET AL.	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communicati n appears on the cover sheet with the correspondence address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *13-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-12 on 5/17/2004 is acknowledged.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guterman et al. (5,712,180).

Regarding claim 1, Guterman et al. teach in figure 12 and related text (column 24, line 18 to column 25, line 24) a method for forming at least one non-volatile memory cell, comprising:

forming a component stack of the at least one non-volatile memory cell on a surface of a substrate, wherein the component stack comprises an electron trapping layer;

forming a dielectric layer over the device;

removing a portion of the dielectric layer 1110 such that a remainder of the dielectric layer exists substantially along sidewalls of the component stack;

forming an oxide layer 1115 over a bit line existing in the substrate adjacent to the component stack; and

forming a first electrically conductive layer POLY3 over the component stack and the oxide layer.

Although Guterman et al. teach in figure 12 and related text forming a dielectric layer and reactive ion etching it back down to form sidewall spacers 1110, Guterman et al. do not explicitly state that the dielectric layer is formed over the component stack. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the dielectric layer over the entire component stack of Guterman et al.'s device before etching the dielectric layer in order to simplify the processing steps of making the device.

Regarding claims 2 and 3, Guterman et al. teach in figure 12 and related text the forming of an oxide layer over a bit line comprises growing an oxide layer over a bit line existing in the substrate adjacent to the component stack, wherein the remainder of the dielectric layer substantially prevents the oxide layer from extending under the component stack.

Regarding claim 7, Guterman et al. teach in figure 12 and related text the forming of a component stack comprises: forming a first oxide layer, a nitride layer, a second oxide layer, and a second electrically conductive layer on a surface of a substrate in that order; forming a patterned photoresist layer on the second electrically conductive layer;

and using the patterned photoresist layer as a mask to pattern the second electrically conductive layer, the second oxide layer, the nitride layer, and the first oxide layer.

Claims 8-10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gutman et al. (5,712,180) in view of Chang et al. (5,836,772). Guterman et al. teach in figure 12 and related text (column 24, line 18 to column 25, line 24) a method for forming at least one non-volatile memory cell, comprising:

forming a first oxide layer, a nitride layer (an electron trapping layer), a second oxide layer 1103, and a first electrically conductive layer 1104 on a surface of a substrate in that order;

forming a patterned photoresist layer 1108 on the first electrically conductive layer;

using the patterned photoresist layer as an etching mask to form a component stack of the at least one non-volatile memory cell on the surface of the substrate;

using a patterned photoresist layer as a doping mask to form a bit line in the substrate adjacent to the component stack;

removing the patterned photoresist layer;

forming a dielectric layer over the device;

removing a portion of the dielectric layer such that a remainder of the dielectric layer 1110 exists substantially along sidewalls of the component stack;

forming/growing an oxide layer 1115 over the bit line; and

forming an electrically conductive layer POLY 3 over the component stack and the oxide layer,

wherein the remainder of the dielectric layer substantially prevents the oxide layer from extending under the component stack.

Although Guterman et al. teach in figure 12 and related text forming a dielectric layer and reactive ion etching it back down to form sidewall spacers 1110, Guterman et al. do not explicitly state that the dielectric layer is formed over the component stack. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the dielectric layer over the entire component stack of Guterman et al.'s device before etching the dielectric layer in order to simplify the processing steps of making the device.

Guterman et al. do not teach using the patterned photoresist layer as a doping mask to form a bit line.

Chang et al. teach in figure 5 and related text using the patterned photoresist layer 28, 30 as an etching mask and as a doping mask to form a bit line 38. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the patterned photoresist layer as an etching mask and as a doping mask to form a bit line in Guterman et al.'s device in order to simplify the processing steps of making the device by using one patterned photoresist layer as an etching mask and as a doping mask.

Regarding claim 12, Guterman et al. and Chang et al. teach the using of the patterned photoresist layer as an etching mask and the using of the patterned photoresist layer as a doping mask comprise: using the patterned photoresist layer as an etching mask to pattern the first electrically conductive layer, the second oxide layer, and the nitride layer; using the patterned photoresist layer as a doping mask to selectively introduce dopant atoms into the surface of substrate; and using the patterned photoresist layer as an etching mask to pattern the first oxide layer.

Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gutman et al. (5,712,180) in view of Applicant Admitted Prior Art (AAPA).

Gutman et al. teach substantially the entire claimed structure, as applied to claim 1 above, except using the silicon nitride as an electron trapping layer. AAPA teaches in figure 1A using the silicon nitride as an electron trapping layer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the silicon nitride as a electron trapping layer in Guterman et al.'s device in order to improve the characteristics of the device by improving its memory holding capabilities.

Regarding claims 5 and 6, Guterman et al. and Chang et al. teach a component stack comprises a first dielectric layer and a second dielectric layer, and wherein the electron trapping layer is interposed between the first and second dielectric layers, and a second

electrically conductive layer, and wherein the electron trapping layer is positioned between the second electrically conductive layer and the surface of the substrate.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gutman et al. (5,712,180) and Chang et al., as applied to claim 8 above, and further in view of Applicant Admitted Prior Art (AAPA).

Gutman et al. and Chang et al. teach substantially the entire claimed structure, as applied to claim 1 above, except using the silicon nitride as an electron trapping layer. AAPA teaches in figure 1A using the silicon nitride as an electron trapping layer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the silicon nitride as a electron trapping layer in Guterman et al. and Chang et al.'s device in order to improve the characteristics of the device by improving its memory holding capabilities.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722

and 308-7724. The Group 2811 Fax Cent r is to be used only for papers related to Group 2811 applicati ns.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday. Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956.**

O.N.
5/24/04

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800